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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,307	02/10/2004	Ching-Nan Hsiao	10113741	1517

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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,307	HSIAO ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the amendment filed on 24 December 2005.

2. The amendment filed on 24 December 2005, canceled claims 13-20.

Accordingly, claims 1-12 are currently pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. *Claims 1-6 and 8-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Hsiao et al. (US 2004/0094781 A1).*[1]

The applied reference has a common assignee and at least one common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference

[1] The Hsiao et al. application publication was cited, but not relied upon, in the previous Office action mailed on 24 August 2005.

was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

The Hsiao et al. application publication (Hsiao) discloses a method for fabricating a multi-bit vertical memory cell (figs. 2a-2f and accompanying text). The method comprises: providing a semiconductor substrate 200 having a trench 208 (fig. 2b and par. 0019, lines 8-11); forming doped areas 214, acting as bit lines, in the semiconductor substrate near its surface and the bottom of the trench (fig. 2d and par. 0021, lines 6-8); forming bit line insulating layers 216 over each of the doping areas (fig. 2e and par. 0022, lines 1-2); forming an insulating layer 220 over a sidewall of the trench and the bit line insulating layers to locally store electric charge (fig. 2e; par. 0023, lines 1-4; and par. 0023, lines 11-13); and forming a conducting layer 224 over the insulating layer and filling in the trench (fig. 2f and par. 0024, lines 1-3).

The method of forming the doping areas comprises: forming a spacer 212 over the sidewall of the trench (fig. 2d and par. 0021, lines 1-3); performing ion implantation in the substrate using the spacer as a mask (fig. 2d and par. 0021, lines 3-6); and removing the spacer, as recited in claim 2 (fig. 2e and par. 0022, lines 5-7).

The spacer 212 is silicon nitride, as recited in claim 3 (par. 0020, line 10 - par. 0021, line 3).

Phosphorus ions are implanted, as recited in claim 4 (par. 0021, lines 3-6).

The bit line insulating layers 216 are formed by thermal oxidation, as recited in claim 5 (par. 0022, lines 1-2).

The thickness of the bit line insulating layers 216 is 300 to 2000 Å, as recited in claim 6 (par. 0022, lines 2-5).

The thickness of the insulating layer 220 is 50 to 110 Å, as recited in claim 8 (par. 23, lines 6-8).

A gate dielectric layer 218 is formed between the insulating layer 220 and the trench surface, as recited in claim 9 (fig. 2e and par. 0023, lines 1-6).

The gate dielectric layer 218 is a gate oxide layer, as recited in claim 10 (par. 0023, lines 1-6).

The gate dielectric layer 218 can have a thickness of 50 Å, as recited in claim 11 (par. 0023, lines 6-8).

The conducting layer 224 is a poly layer, as recited in claim 12 (par. 0024, lines 1-3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. *Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsiao et al. (US 2004/0094781 A1) in view of Forbes US 6,853,587 B2).*

As explained above, Hsiao discloses forming an insulating layer 220 over a sidewall of the trench and the bit line insulating layers to locally store charge. However, Hsiao does not teach that the insulating layer 220 is a silicon-rich oxide (SRO) layer. Instead, the insulating layer 220 is a silicon nitride layer (par. 0023, lines 4-6). The silicon nitride layer 220 is sandwiched between two silicon oxide layers 218 and 222, thereby, forming an oxide-nitride-oxide (ONO) layer 223 (par. 0023, lines 4-6).

The Forbes patent (Forbes) discloses a method for forming a vertical memory cell (fig. 3A; col. 7, line 60 - col. 8, line 30; and col. 9, lines 39-44), which may form part of a multi-bit vertical memory cell as shown in figure 4A. In one preferred embodiment, the vertical memory cell comprises an oxide-nitride-oxide (ONO) layer 307, wherein the nitride layer is used to locally store charge (fig. 3A; col. 8, lines 9-11; and col. 9, lines 39-44). In an alternate embodiment, a silicon-rich oxide layer may be used in place of the ONO layer (col. 8, lines 11-15).

Hsiao and Forbes are from the same field of endeavor, namely vertical NROM (nitride read-only-memory) cells and methods of fabricating the same. Therefore, the purpose for which Forbes is relied upon in this rejection would have been recognized in the prior art reference to Hsiao by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Hsiao by replacing the ONO composite layer

223 with a silicon-rich oxide layer (SRO), as taught by Forbes, because: the SRO layer requires only a single coating step, whereas the ONO layer requires at least three separate coating steps (e.g. a thermal oxidation step to grow the oxide layer 218 followed by two separate chemical vapor deposition steps to form the silicon nitride layer 220 and the silicon oxide layer 222, respectively). In other words, the formation of an SRO layer requires fewer process steps than the formation of an ONO layer which, in turn, reduces the total number of process steps needed to form the multi-bit vertical memory cell, thereby, simplifying the fabrication process.

Response to Arguments

5. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

6. The amendment filed on 24 December 2005 has overcome the rejection of claims 1-12 under 35 USC 112, second paragraph, as set forth in the Office action mailed on 24 August 2005. Accordingly, the rejection is withdrawn.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Toniae M. Thomas
Patent Examiner
Technology Center 2800

TMT
16 March 2006